AD8313 Evaluation Board

EVAL-AD8313EB

BOARD DESCRIPTION

Schematic and Layout

Figure 5 shows the schematic of the evaluation board that was used to characterize the AD8313. Note that uninstalled components are drawn in as dashed.

This is a 3-layer board (signal, ground, and power), with a Duroid dielectric (RT 5880, h = 5 mil, ε_R = 2.2). FR4 can also be used, but microstrip dimensions must be recalculated because of the different dielectric constant and board height. The trace layout and silkscreen of the signal and power layers are shown in Figures 1 to 4. A detail of the PCB footprint for the MSOP package and the pads for the matching components are shown in Figure 6.

The vacant portions of the signal and power layers are filled out with ground plane for general noise suppression. To ensure a low impedance connection between the planes, there are multiple through-hole connections to the RF ground plane. While the ground planes on the power and signal planes are used as general-purpose ground returns, any RF grounds related to the input matching network (e.g., C2) are returned directly to the RF internal ground plane.

General Operation

The board should be powered by a single supply in the range, 2.7 V to 5.5 V. The power supply to each of the VPOS pins is decoupled by a 10 Ω resistor and a 0.1 μF capacitor.

The two signal inputs are ac-coupled using 680 pF high quality RF capacitors (C1, C2). A 53.6 Ω resistor across the differential signal inputs (INHI, INLO) combines with the internal 900 Ω input impedance to give a broadband input impedance of 50.6 Ω. This termination is not optimal from a noise perspective due to the Johnson noise of the 53.6 Ω resistor; neither does it take account for the AD8313's reactive input impedance or of the decrease over frequency of the resistive component of the input impedance. However, it does allow evaluation of the AD8313 over its complete frequency range without having to design multiple matching networks.

For optimum performance, a narrow-band match can be implemented by replacing the 53.6 Ω resistor (labeled L/R) with an RF inductor and replacing the 680 pF capacitors with appropriate values. The Input Matching section in the AD8313 data sheet includes a table of recommended values for selected frequencies and explains the method of calculation.

Switch 1 is used to select between power-up and power-down modes. Connecting the PWDN pin to ground enables normal operation of the AD8313. In the opposite position, the PWDN pin can either be driven externally (SMA connector labeled EXT ENABLE) to either device state or allowed to float to a disabled device state.

The evaluation board ships with the AD8313 configured to operate in RSSI measurement mode, the logarithmic output appearing on the SMA connector labeled VOUT. This mode is set by the 0 Ω resistor (R11), which shorts the VOUT and VSET pins to each other.

Varying the Logarithmic Slope

The slope of the AD8313 can be increased from its nominal value of 18 mV/dB to a maximum of 40 mV/dB by removing R11, the 0 Ω resistor, which shorts VSET to VOUT. VSET and VOUT are now connected through a 20 kΩ potentiometer.

Operating in Controller Mode

To put the AD8313 into controller mode, R7 and R11 should be removed, breaking the link between VOUT and VSET. The VSET pin can then be driven externally via the SMA connector labeled EXT VSET IN ADJ.

Increasing Output Current

To increase the output current of VOUT, set both R3 and R11 to 0 Ω and install potentiometer R4 (1 kΩ to 5 kΩ).

ORDERING GUIDE

Model	Package Description
AD8313-EVAL	Evaluation Board

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the EVAL-AD8313EB features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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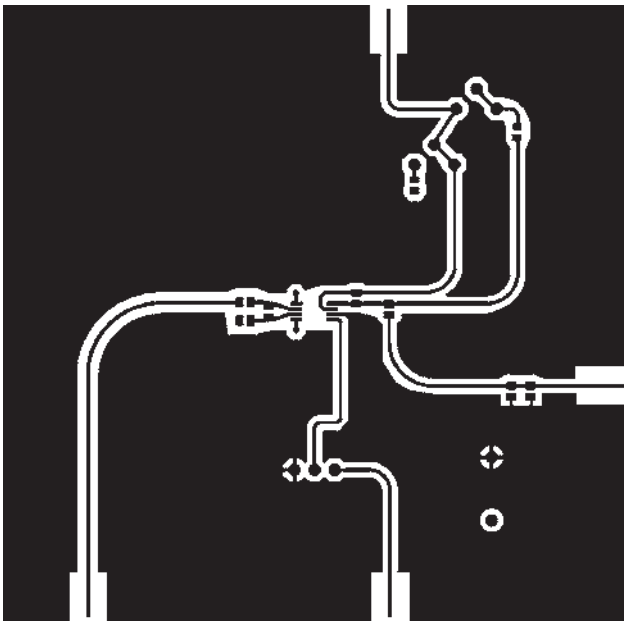

Figure 1. Layout of Signal Layer

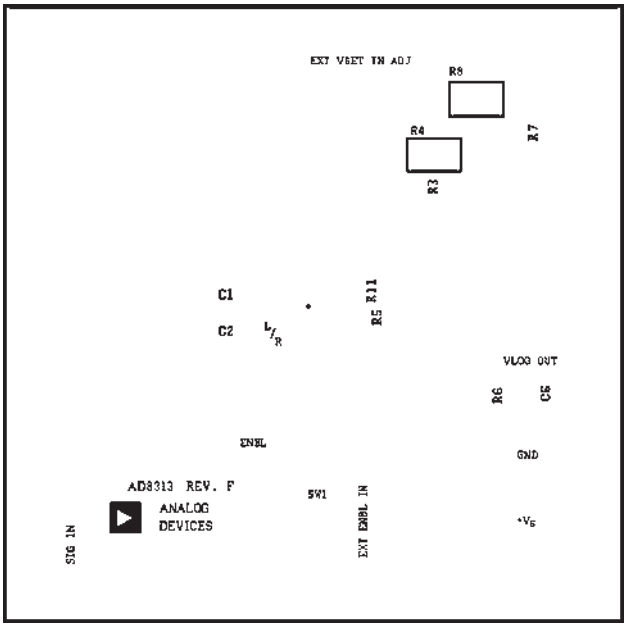

Figure 3. Signal Layer Silkscreen

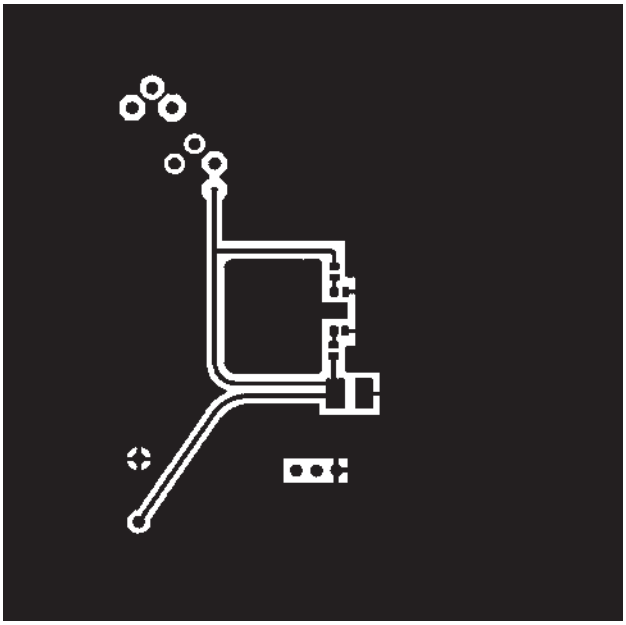

Figure 2. Layout of Power Layer

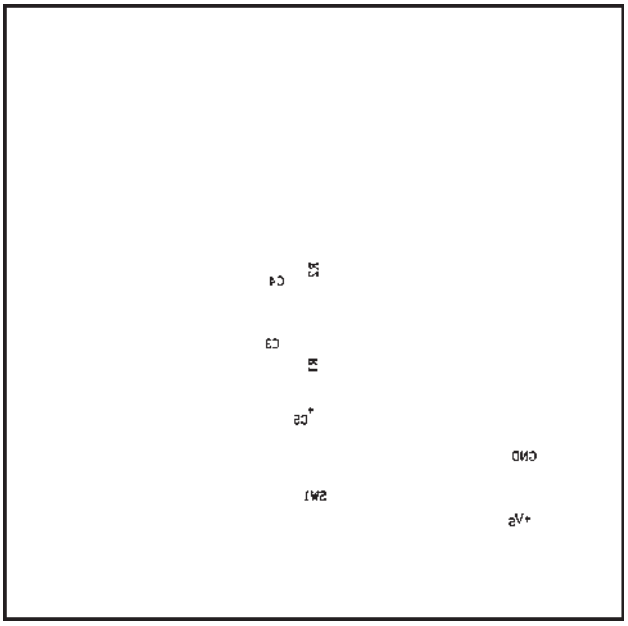

Figure 4. Power Layer Silkscreen

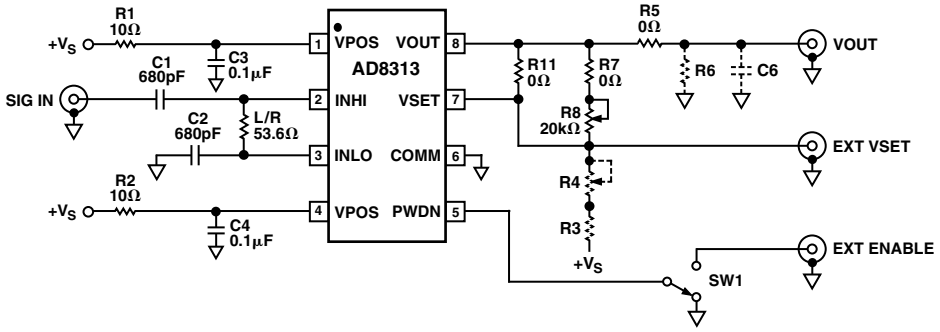

Figure 5. Evaluation Board Schematic

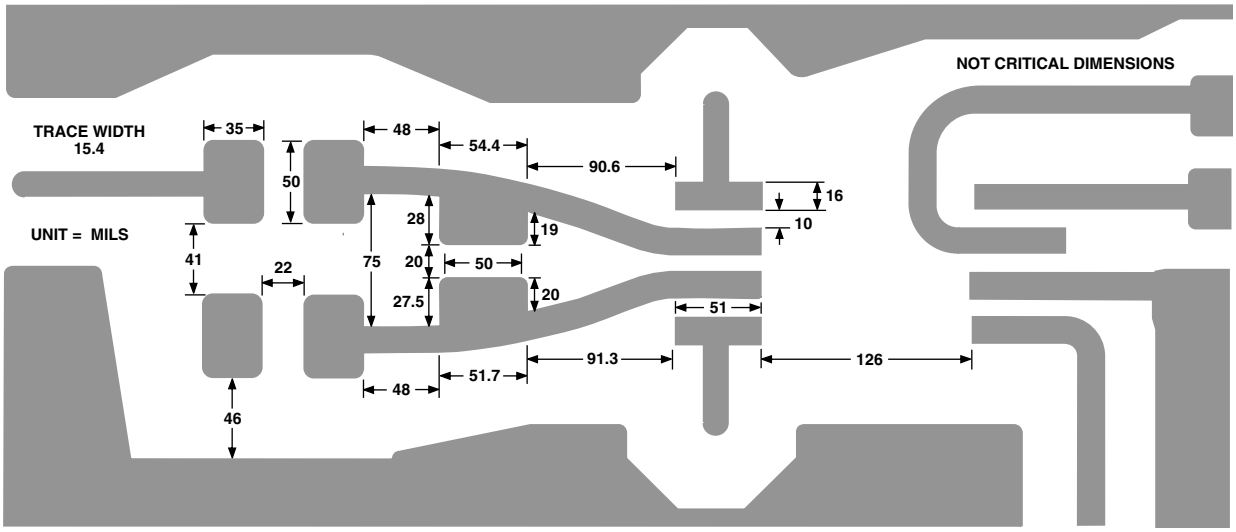

Figure 6. Detail of PCB Footprint for Package and Pads for Matching Network

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